1 PRODUCT OVERVIEW

CALMRISC OVERVIEW

The S3CB018/FB018 single-chip CMOS microcontroller is designed for high performance using Samsung's newest 8-bit CPU core, CalmRISC.

CalmRISC is an 8-bit low power RISC microcontroller. Its basic architecture follows Harvard style, that is, it has separate program memory and data memory. Both instruction and data can be fetched simultaneously without causing a stall, using separate paths for memory access. Represented below is the top block diagram of the CalmRISC microcontroller.

S3CB018/FB018 OVERVIEW

FEATURES SUMMARY

CPU

- 8-Bit RISC architecture

Memory

- ROM: 4 Kword (8 K-byte)
- RAM: 3072 (1024+2048) byte
  1024 (X-memory) byte
  2048 (Y-memory) byte

Stack

- size: maximum 16 (word)-level

26 I/O Pins

- I/O: 26 pins, including 8 S/W open drain pins

8-Bit Basic Timer

- Programmable interval timer
- 8 kinds of clock source

Watchdog Timer

- System reset when 11-bit counter overflows

16-Bit Timer/Counter

- Programmable interval timer
- Two 8-bit timer counter mode and one 16-bit timer counter mode, selectable by S/W

Watch Timer

- Real time clock or interval time measurement
- Four frequency outputs for buzzer sound

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB first or MSB first transmission selectable
- Internal and external clock source

16-Bit Serial I/O Interface

- 16-bit transmit/receive mode
- External clock source

Coprocessor

- MAC 816
- 8 x 16, 16 x 16 Multiply and Accumulation
- Arithmetic operation

Two Power-Down Modes

- Idle mode: only CPU clock stop
- Stop mode: selected system clock and CPU clock stop

Oscillation Sources

- Crystal and Ceramic (0.4-20MHz), RC Oscillation
- Programmable oscillation source

Instruction Execution Times

- 50ns at 20MHz for 1 cycle instruction
- 100ns at 20MHz for 2 cycle instruction

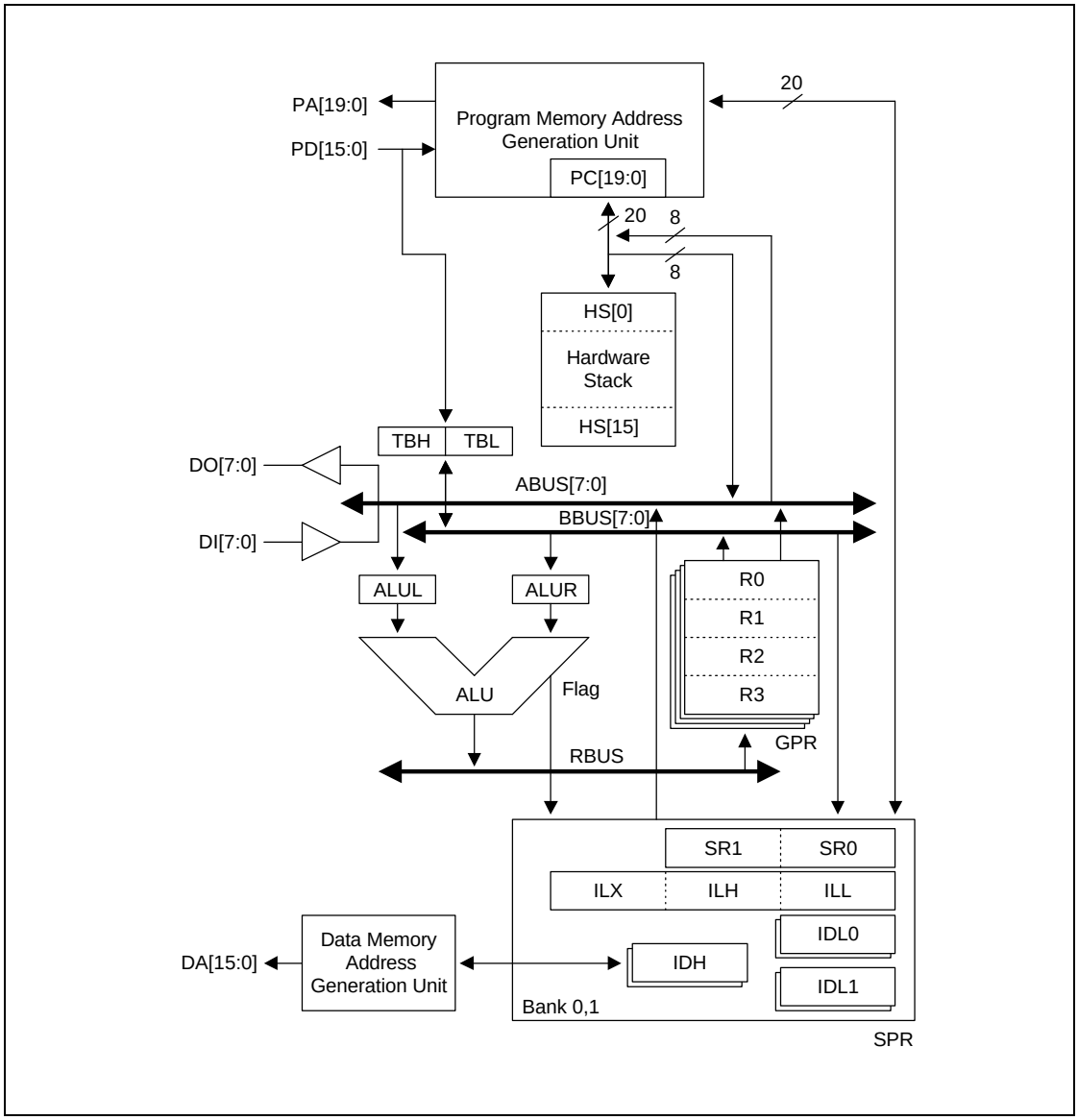


Figure 1-1. Top Block Diagram of CalmRISC

The CalmRISC building blocks consist of:

— An 8-bit ALU
— 16 general purpose registers (GPR)
— 11 special purpose registers (SPR)
— 16-level hardware stack
— Program memory address generation unit
— Data memory address generation unit

16 GPR's are grouped into four banks (Bank0 to Bank3) and each bank has four 8-bit registers (R0, R1, R2, and R3). SPR's, designed for special purposes, include status registers, link registers for branch-link instructions, and data memory index registers. The data memory address generation unit provides the data memory address (denoted as *DA[15:0]* in the top block diagram) for a data memory access instruction. Data memory contents are accessed through *DI[7:0]* for read operations and *DO[7:0]* for write operations. The program memory address generation unit contains a program counter, PC[19:0], and supplies the program memory address through *PA[19:0]* and fetches the corresponding instruction through *PD[15:0]* as the result of the program memory access. CalmRISC has a 16-level hardware stack for low power stack operations as well as a temporary storage area.

CalmRISC has a 3-stage pipeline as described below:

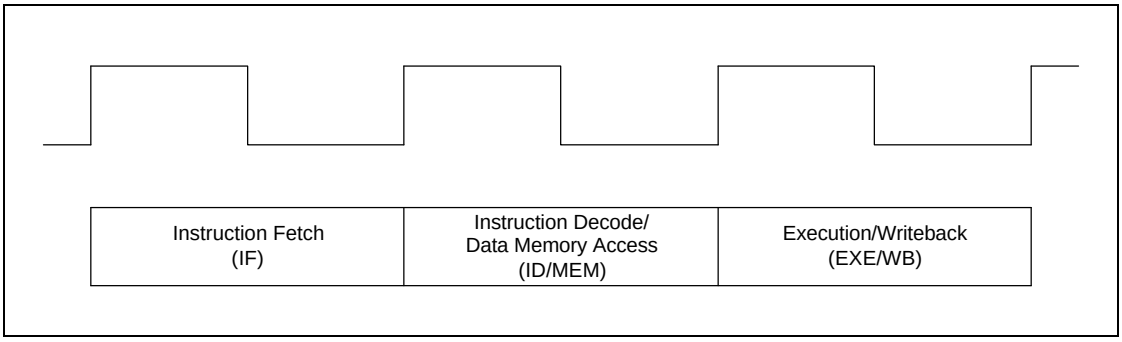


Figure 1-2. CalmRISC Pipeline Diagram

As can be seen in the pipeline scheme, CalmRISC adopts a register-memory instruction set. In other words, data memory where *R* is a GPR, can be one operand of an ALU instruction as shown below:

The first stage (or cycle) is Instruction Fetch stage (IF for short), where the instruction pointed to by the program counter, PC[19:0] , is read into the Instruction Register (IR for short). The second stage is Instruction Decode and Data Memory Access stage (ID/MEM for short), where the fetched instruction (stored in IR) is decoded and data memory access is performed, if necessary. The final stage is Execute and Write-back stage (EXE/WB), where the required ALU operation is executed and the result is written back into the destination registers.

Since CalmRISC instructions are pipelined, the next instruction fetch is not postponed until the current instruction is completely finished, but is performed immediately after the current instruction fetch is done. The pipeline stream of instructions is illustrated in the following diagram.

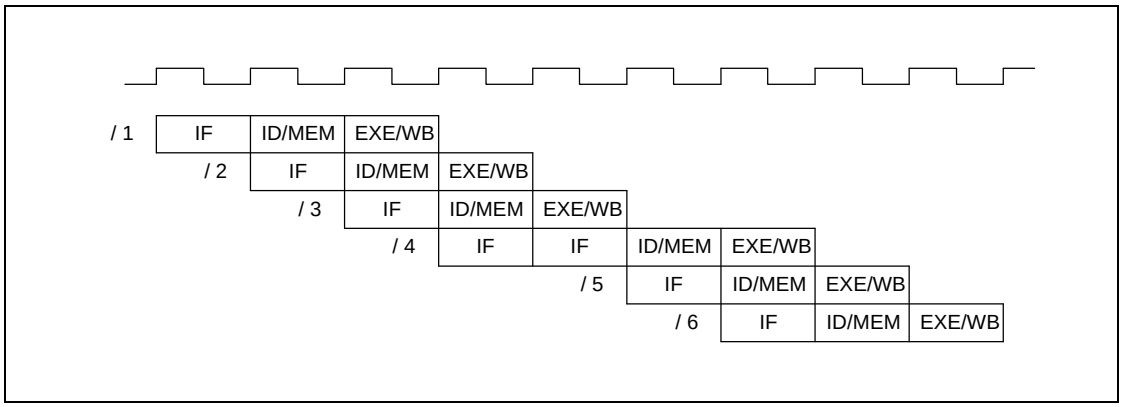


Figure 1-3. CalmRISC Pipeline Stream Diagram

Most CalmRISC instructions are 1-word instructions, while same branch instructions such as “LCALL” and “LJT” instructions are 2-word instructions. In Figure 1-3, the instruction, I_4, is a long branch instruction and it takes two clock cycles to fetch the instruction. As indicated in the pipeline stream, the number of clocks per instruction (CPI) is 1 except for long branches, which take 2 clock cycles per instruction.

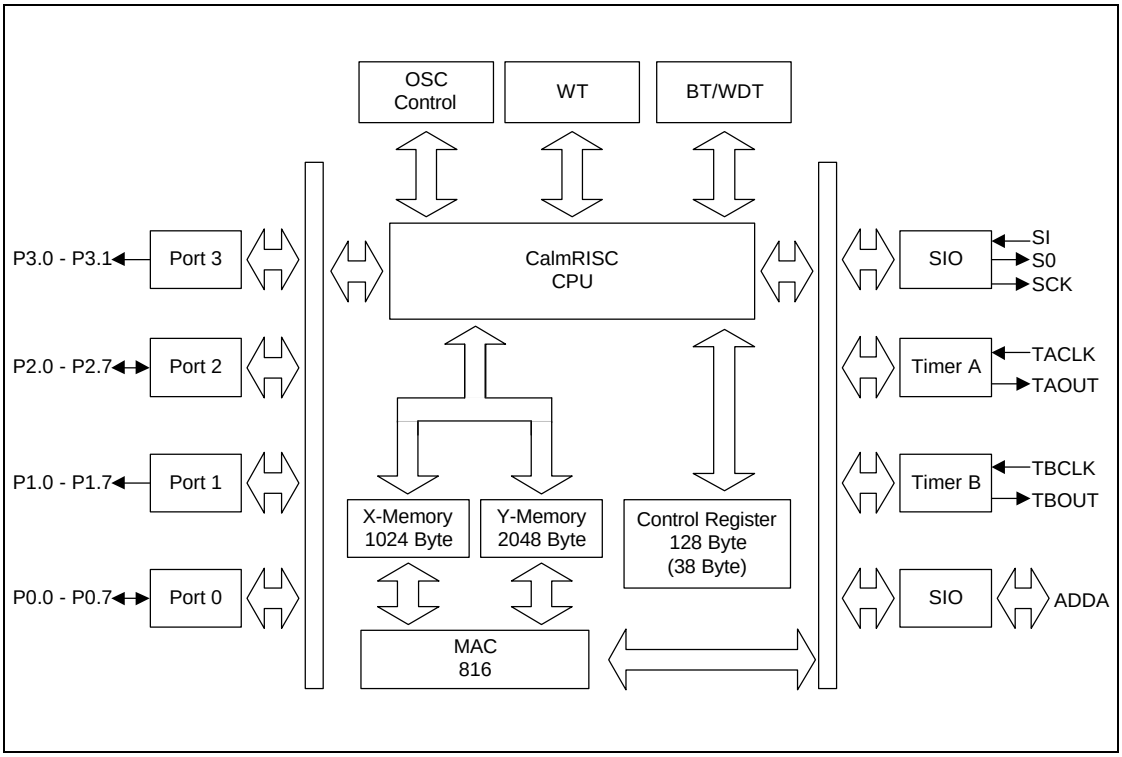


Figure 1-4. S3CB018/FB018 Block Diagram

PIN ASSIGNMENTS

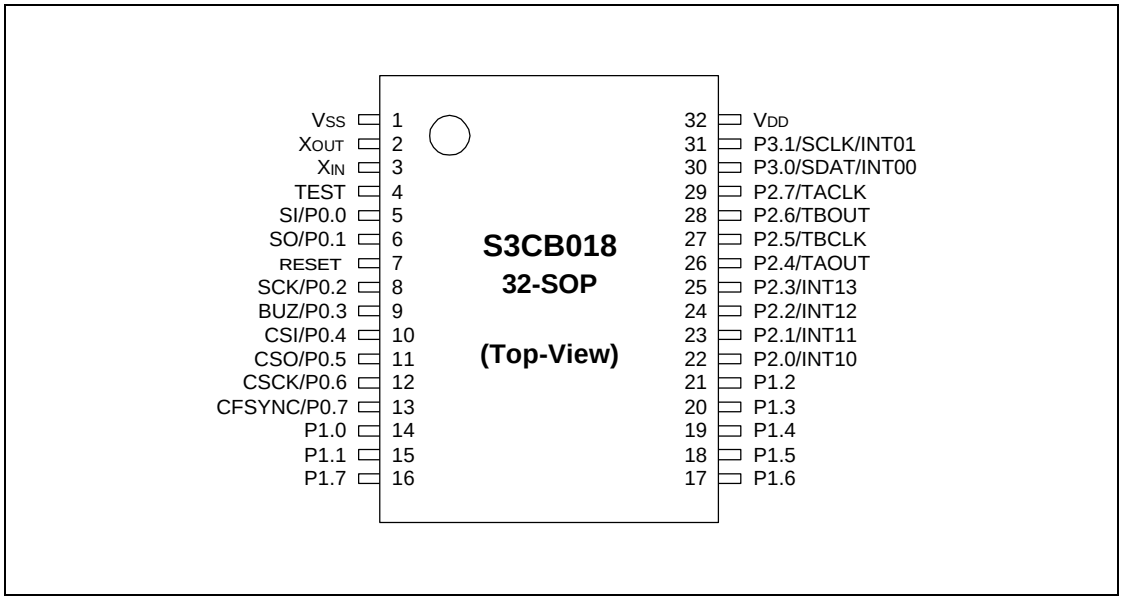


Figure 1-5. 32-SOP Pin Assignment

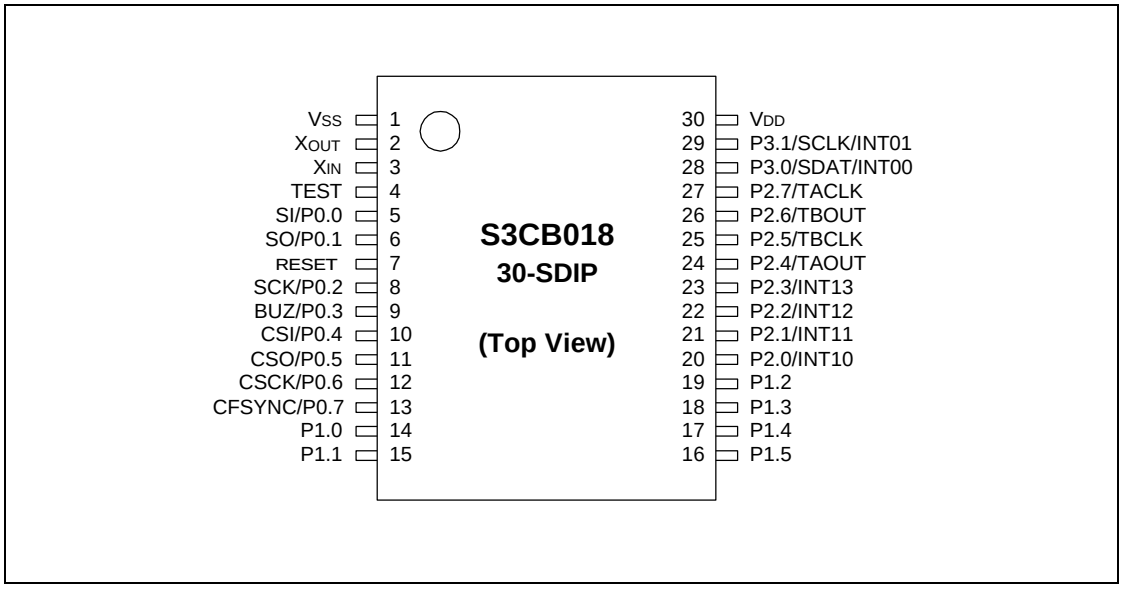


Figure 1-6. 30-SDIP Pin Assignment

I/O PIN DESCRIPTION

Table 1-1. S3CB018/FB018 Pin Descriptions (32-SOP)

Pin Name	Pin Type	Pin Description	Circuit Type	Share Pins
P0.0-P0.7	I/O	I/O port with bit programmable pins; Input and output mode are selectable by software; Software assignable pull-up. P0.4-P0.7 can be used as inputs for comparator input CIN0-CIN3.; Alternately they can be used as SI, SO, SCK, BUZ, CSI, CSO, CSCK, CFSYNC.	D-2 F-10	SI, SO, SCK BUZ, CSI, CSO, CSCK, CFSYNC
P1.0-P1.7	O	Output port with bit programmable pins; Push-pull output mode and open-drain output mode are selected by software; Software assignable pull-up.	E-2	
P2.0-P2.7	I/O	I/O port with bit programmable pins; Input and output mode are selectable by software; Software assignable pull-up; P2.0-P2.3 can be used as inputs for external interrupts INT10-INT13. (with noise filter) ; Alternately they can be used as TAOUT, TACLK or TBOUT, TBCLK.	D-4 D-2	INT10-INT13 TAOUT TACLK TBOUT TBCLK
P3.0-P3.1	I/O	I/O port with bit programmable pins; Input or output mode selected by software; software assignable pull-up; P3.0-P3.1 can be used as inputs for external interrupts INT00-INT01. (with noise filter and interrupt polarity control)	D-4	INT00-INT01

Table 1-2. S3CB018/FB018 Pin Descriptions (30-SDIP)

Pin Name	Pin Type	Pin Description	Circuit Type	Share Pins
P0.0-P0.7	I/O	I/O port with bit programmable pins; Input and output mode are selectable by software; Software assignable pull-up. P0.4-P0.7 can be used as SI, SO, SCK, BUZ, CSI, CSO, CSCK, CFSYNC, Alternately.	D-2 F-10	SI, SO, SCK BUZ, CSI, CSO, CSCK, CFSYNC
P1.0-P1.5	O	O port with bit programmable pins; Push-pull output mode and open-drain output mode are selected by software; Software assignable pull-up.	E-2	
P2.0-P2.7	I/O	I/O port with bit programmable pins; Input and output mode are selectable by software; Software assignable pull-up; P2.0-P2.3 can be used as inputs for external interrupts INT10-INT13. (with noise filter); Alternately they can be used as TAOUT, TACLK or TBOUT, TBCLK.	D-4 D-2	INT10-INT13 TAOUT TACLK TBOUT TBCLK
P3.0-P3.1	I/O	I/O port with bit programmable pins; Input or output mode selected by software; software assignable pull-up; P3.0-P3.1 can be used as inputs for external interrupts INT00-INT01. (with noise filter and interrupt polarity control)	D-4	INT00-INT01

NOTE: In S3CB018/FB018, the CSI, CSO, CSCK, CFSYNC pins are shared with P0.7-P0.4.

Table 1-3. I/O Pin Description

Pin Name	Pin Type	Description
CSI	I	AD/DA Serial Input (from codec)
CSO	O	AD/DA Serial Output (to codec)
CSCK	I	AD/DA Serial Clock (from codec)
CFSYNC	I	AD/DA Sync signal (from codec)
SI	I/O	Serial data input
SO	I/O	Serial data output
SCK	I/O	Serial I/O interface clock signal
BUZ	I/O	0.5 kHz, 1 kHz, 2 kHz, or 4 kHz frequency output at 4.19 MHz for buzzer sound
INT10-INT13	I	External interrupts. Stop release. Can't be masked by S/W individually but wholly.
TAOUT	I/O	Timer A interval mode output
TACLK	I/O	Timer A counter external clock input
TBOUT	I/O	Timer B interval mode output
TBCLK	I/O	Timer B counter external clock input
INT00-INT01	I	External interrupts. Stop release. Can be masked by S/W individually.
SDAT	I	Serial data for Programmable memory
SCLK	I	Serial clock for Programmable memory
VDD	–	Power supply
VSS	–	Ground
TEST	–	Test signal input
RESET	I	Reset signal
X_{IN}, X_{OUT}	–	Crystal, ceramic and RC oscillator signal for system clock (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT})

PIN ASSIGNMENTS

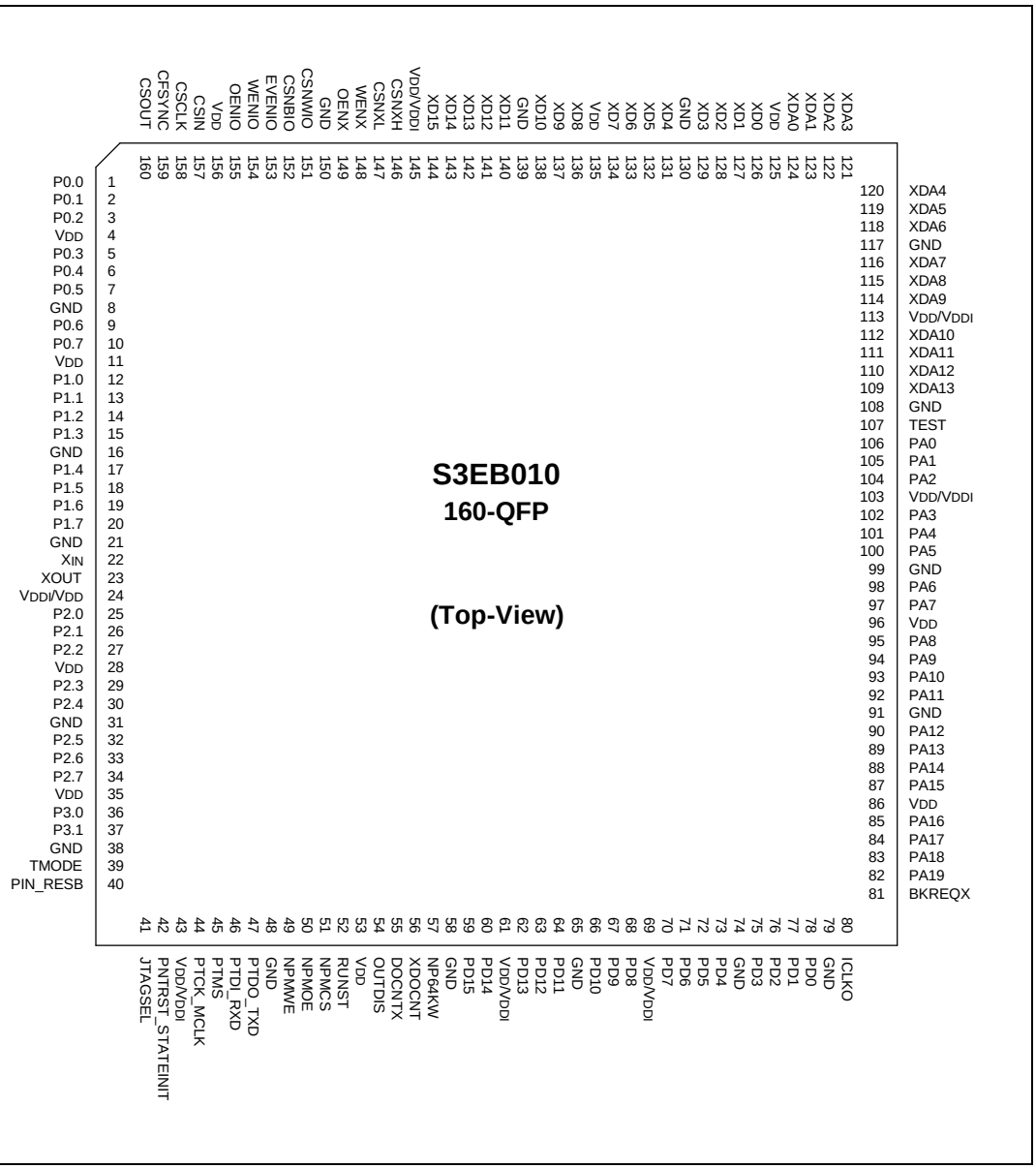


Figure 1-7. S3EB010 Pin Diagram

Table 1-4. Evaluation Chip Pin Descriptions

No.	Pin Name	Pin Type	Description
1-3 5-9	P0.0-P0.2 P0.3-P0.7	I/O	Port 0
12-15 17-20	P1.0-P1.3 P1.4-P1.7	O	Port 1
22	X_{IN}	I	Clock In
23	X_{OUT}	O	Clock Out
25-27 29, 30 32, 34	P2.0-P2.2 P2.3, P2.4 P2.5-P2.7	I/O	Port 2
36, 37	P3.0, P3.1	I/O	Port 3
39	TMODE	I	Test Mode pin; 1: skip warm-up time, 0: normal mode
40	PIN_RESB	I	Asynchronous reset, active low
41	JTAGSEL	I	JTAG mode select; 1: parallel, 0: serial
42	PNTRST_STSTEINIT	I	JTAG/UART pin
44	PTCK_MCLK	I	JTAG/UART pin
45	PTMS	I	JTAG/UART pin
46	PTDI_RXD	I	JTAG/UART pin
47	PTDO_TXD	O	JTAG/UART pin
49	NPMWE	O	Program Memory Write Enable, active low
50	NPMOE	O	Program Memory Output Enable, active low
51	NPMCS	O	Program Memory Chip Select, active low
52	RUNST	O	Run Status Indicator
54	OUTDIS	I	I/O PAD Disable for debugger
55	DOCNTX	I	Data Bus Output Control
56	XDOCNTX	I	External X-Memory Data Bus Output Control
57	NPM64KW	I	Up to 64KW Program Memory, active low
59, 60 62-64 66-68 70-73 75-78	PD15-PD14 PD13-PD11 PD10-PD8 PD7-PD4 PD3-PD0	I/O	Program Memory Data Bus

Table 1-4. Evaluation Chip Pin Descriptions (Continued)

No.	Pin Name	Pin Type	Description
80	ICLKO	O	ICLK Output
81	BKREQX	I	Break input for debugger
82-85 87-90 92-95 97, 98 100-102 104-106	PA19-PA16 PA15-PA12 PA11-PA8 PA7, PA6 PA5-PA3 PA2-PA0	O	Program Memory Address
107	TEST	I	Test pin for debugger
109-112 114-116 118-124	XDA13-XDA10 XDA9-XDA7 XDA6-XDA0	O	External X-Memory Address
126-129 131-134 136-138 140-144	XD0-XD3 XD4-XD7 XD8-XD10 XD11-XD15	I/O	External X-Memory Data Bus
146	CSNXH	O	External X-Memory High Byte Chip Select, active low
147	CSNXL	O	External X-Memory Low Byte Chip Select, active low
148	WENX	O	External X-Memory Write Enable, active low
149	OENX	O	External X-Memory Output Enable, active low
151	CSNWIO	O	External I/O Word Chip Select, active low
152	CSNBIO	O	External I/O Byte Chip Select, active low
153	EVENIO	O	External I/O Even Indicator; 1:Even, 0: Odd
154	WENIO	O	External I/O Write Enable, active low
155	OENIO	O	External I/O Output Enable, active low
157	CSIN	I	AD / DA Serial Input (from codec)
158	CSCLK	I	AD / DA Serial Clock (from codec)
159	CFSYNC	I	AD / DA Sync signal (from codec)
160	CSOUT	O	AD / DA Serial Output (to codec)
VDD	Power supply	–	4, 11, 24, 28, 35, 43, 53, 61, 69, 86, 96, 103, 113 125, 135, 145, 156
GND	Ground	–	8, 16, 21, 31, 38, 48, 58, 65, 74, 79, 91, 99, 108, 117 130, 139, 150

PIN CIRCUIT DIAGRAMS

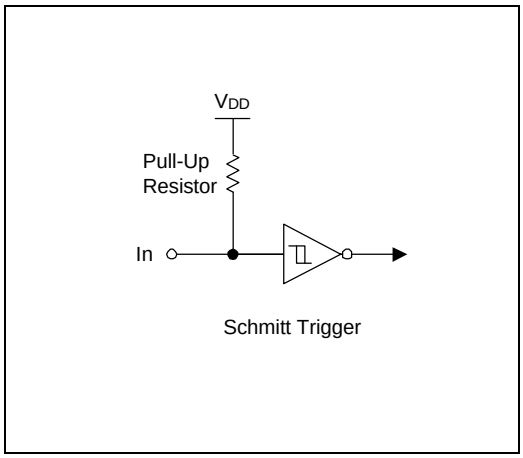


Figure 1-8. Pin Circuit Type B (RESET)

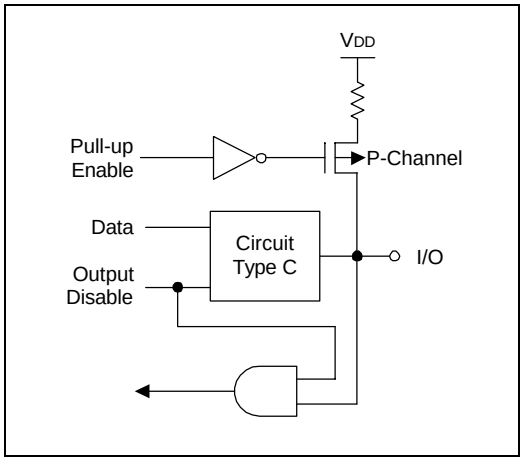


Figure 1-10. Pin Circuit Type D-2 (P0.0-P0.3, P2.4-P2.7)

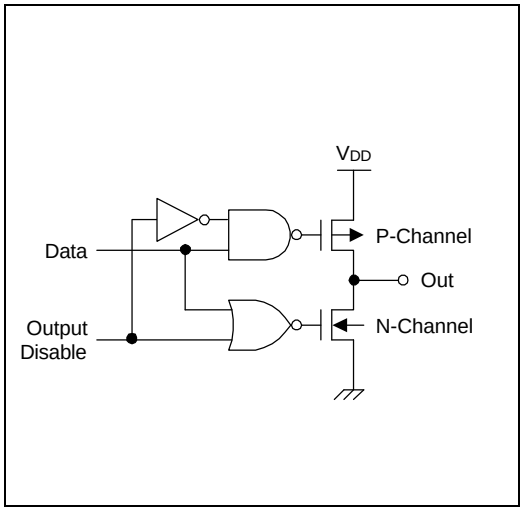


Figure 1-9. Pin Circuit Type C

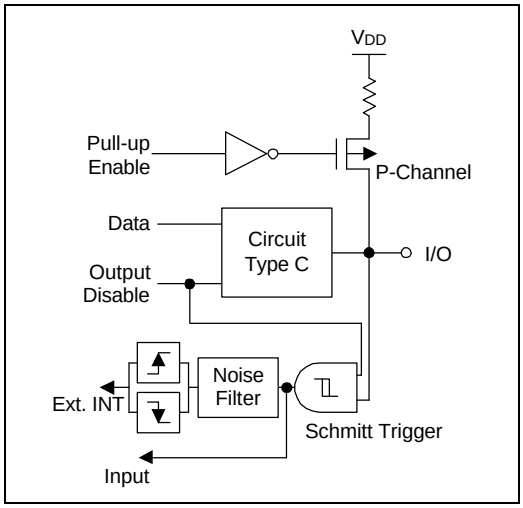


Figure 1-11. Pin Circuit Type D-4 (P2.0-P2.3, P3)

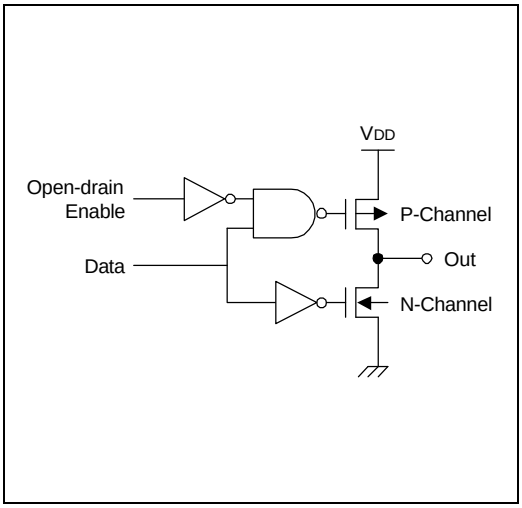


Figure 1-12. Pin Circuit Type E-2 (P1)

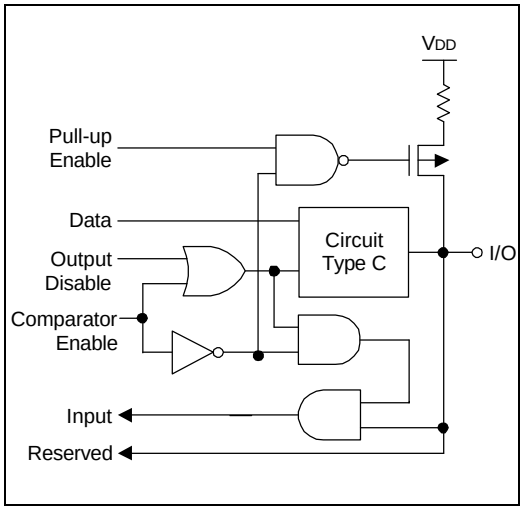


Figure 1-13. Pin Circuit Type F-10 (P0.4-P0.7)

18 ELECTRICAL DATA

OVERVIEW

Table 18-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	–0.3 to + 6.0	V
Input voltage	V_I	–	–0.3 to V_{DD} + 0.3	
Output voltage	V_O	–	–0.3 to V_{DD} + 0.3	
Output current high	I_{OH}	One I/O pin active	–18	mA
		All I/O pins active	–60	
Output current low	I_{OL}	One I/O pin active	+ 30	
		Total pin current for ports 1, 2, 3	+ 100	
Operating temperature	T_A	–	–40 to + 85	°C
Storage temperature	T_{STG}	–	–65 to + 150	

Table 18-2. D.C. Electrical Characteristics

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage (HSX mode)	V_{DD}	F_{CPU} = 20 MHz	4.5	–	5.5	V
		F_{CPU} = 3 MHz	1.8		5.5	
Operating Voltage (MSX mode)	V_{DD}	F_{CPU} = 10 MHz	4.5	–	5.5	
		F_{CPU} = 3 MHz	1.8		5.5	

(T_A = 40° °C, V = 1.8 V to 5.5 V)

Parameter		Conditions	Min		Max	Unit
	V_{IH1}	IH2	0.8 V	–	DD	V
	IH2	X	V_{DD}- 0.1			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	
	V_{IL2}	X_{IN}			0.1	
Output high voltage	V_{OH1}	V_{DD} = 5V; I_{OH} = -1 mA All output pins	V_{DD}-1.0	–	–	V
Output low voltage	V_{OL1}	V_{DD} = 5V; I_{OL} = 8 mA All output pins except V_{OL2}	–		2	
	V_{OL2}	V_{DD} = 5V; I_{OL} = 15 mA, Port 1			2	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	3	uA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, XT_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except I_{LIL2}	–	–	-3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, XT_{IN}, RESET			-20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and Output pins	–	–	3	uA
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and Output pins	–	–	-3	
Oscillator feed back resistors	R_{osc1} (HSX)	V_{DD} = 5.0 V, T_A = 25°C, X_{IN} = V_{DD}, X_{OUT} = 0V	510	710	910	kΩ
	R_{osc2} (MSX)	V_{DD} = 5.0 V,T_A = 25°C, X_{IN} = V_{DD}, X_{OUT} = 0V	510	710	910	
	R_{osc3} (LSX)	V_{DD} = 5.0 V, T_A = 25°C, X_{IN} = V_{DD}, X_{OUT} = 0V	2.0	2.7	3.5	MΩ
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0,1,2,3,4,5 T_A=25°C	30	50	70	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% T_A=25°C, RESET only	110	210	310	

Table 18-2. D.C. Electrical Characteristics (Continued)

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (1)	I_{DD1}(2)	Operating mode: V_{DD} = 5 V ± 10% **20 MHz** crystal oscillator(HSX)	–	10	20	mA
		5 MHz crystal oscillator(MSX)		4	8	
		V_{DD} = 3 V ± 10% **5 MHz** crystal oscillator(MSX)		2	4	
	I_{DD2}(3)	Idle mode: V_{DD} = 5 V ± 10% **20 MHz** crystal oscillator(HSX)	–	2.5	5	mA
		5 MHz crystal oscillator(MSX)		1	2	
		V_{DD} = 3 V± 10% **5 MHz** crystal oscillator(MSX)		0.4	0.8	
	I_{DD3}	Stop mode V_{DD} = 5 V ± 10%	–	0.5	3	uA
		V_{DD} = 3 V ± 10%		0.2	1.2	

NOTES:
1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. In operating current test mode Timer A and Timer B are running.
3. In idle current test mode the Watch timer is running.
4. The operating and idle currents are measured at weak mode.

Table 18-3. A. C. Electrical Characteristics

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t_{INTH}, t_{INTL}	P2.0 - P2.3, P3.0 - P3.1 V_{DD} = 5V	200	–	–	ns
RESET input low width	t_{RSL}	V_{DD} = 5V ± 10%	1	–	–	us

NOTE: User must keep a value larger than the min value.

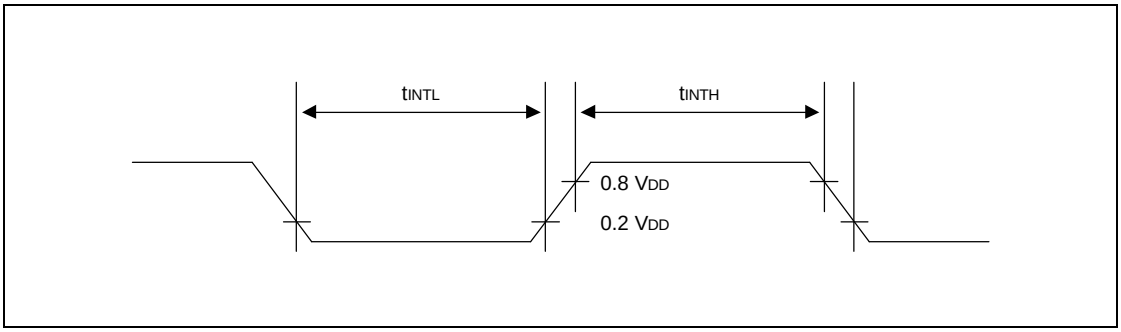


Figure 18-1. Input Timing for External Interrupts

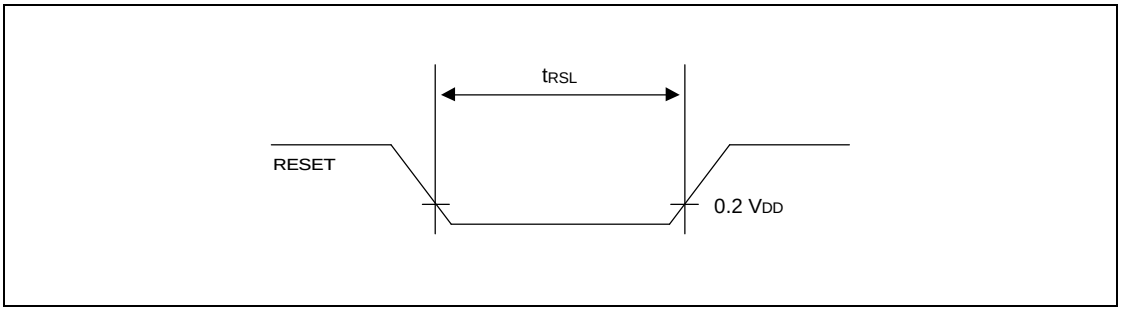


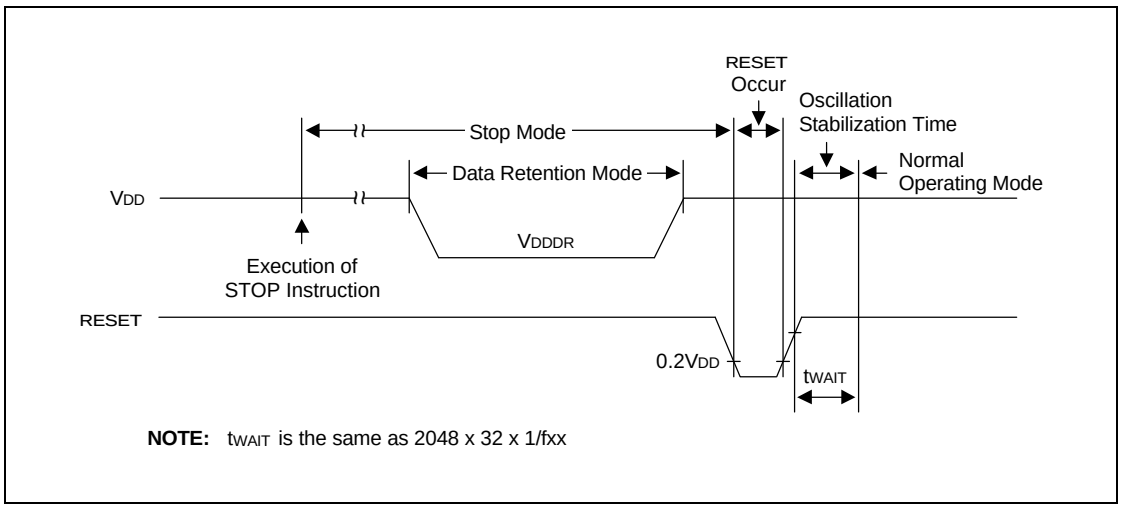
Figure 18-2. Input Timing for RESET

Table 18-4. Data Retention Supply Voltage in Stop Mode

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5V)

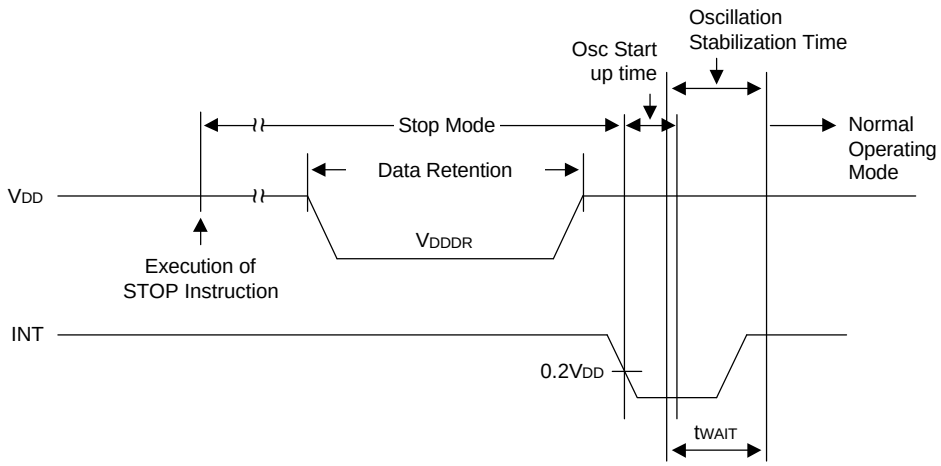
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		1.5	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.5V	–	–	2	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.



NOTE: t_{WAIT} is the same as 2048 x 32 x 1/fxx

Figure 18-3. Stop Mode Release Timing When Initiated by a RESET



NOTE: t_{WAIT} is the same as 2048 x 32 x 1/fxx. The value of 2048 which is selected for the clock source of the basic timer counter can be changed. Then the value of t_{WAIT} will be changed and ,when you select 16 instead of 32, the value of twait will also be changed.

Figure 18-4. Stop Mode Release Timing When Initiated by Interrupts

Table 18-5. Synchronous SIO Electrical Characteristics

(T_A = –40°C to + 85°C V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V, fxx = 10 MHz oscillator)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK Cycle time	t_{CYC}	–	200	–	–	ns
Serial Clock High Width	t_{SCKH}	–	60	–	–	
Serial Clock Low Width	t_{SCKL}	–	60	–	–	
Serial Output data delay time	t_{OD}	–	–	–	50	
Serial Input data setup time	t_{ID}	–	40	–	–	
Serial Input data Hold time	t_{IH}	–	100	–	–	

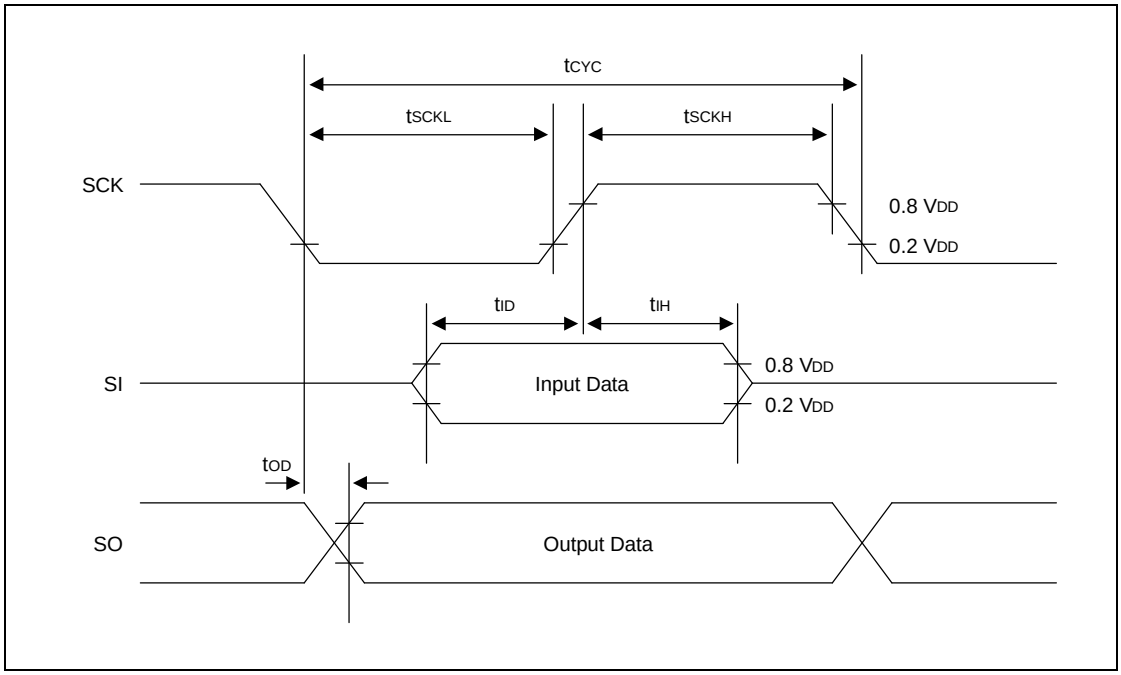
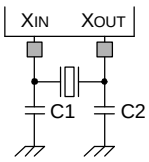
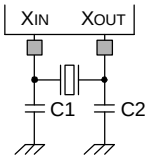
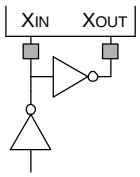


Figure 18-5. Serial Data Transfer Timing

Table 18-6. Main Oscillator Frequency

(T_A = -40°C + 85°C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		LSX mode	32	32.768	35	kHz
		MSX mode	0.4	–	10	MHz
		HSX mode	0.4	–	20	
Ceramic		LSX mode	32	32.768	35	kHz
		MSX mode	0.4	–	10	MHz
		HSX mode	0.4	–	20	
External clock		LSX mode	32	32.768	35	kHz
		MSX mode	0.4	–	10	MHz
		HSX mode	0.4	–	20	
RC		r = 22Kohm, V_{DD} = 5 V Direct soldering	1.4	2	2.6	MHz

NOTES:

1. Keep the wiring length as short as possible.
2. Do not cross the wiring with the other signal lines.
3. Do not route the wiring near a signal line through which a high fluctuating current flows.
4. Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
5. Do not ground the capacitor to a ground pattern through which a high current flows.
6. Do not fetch signals from the oscillator.

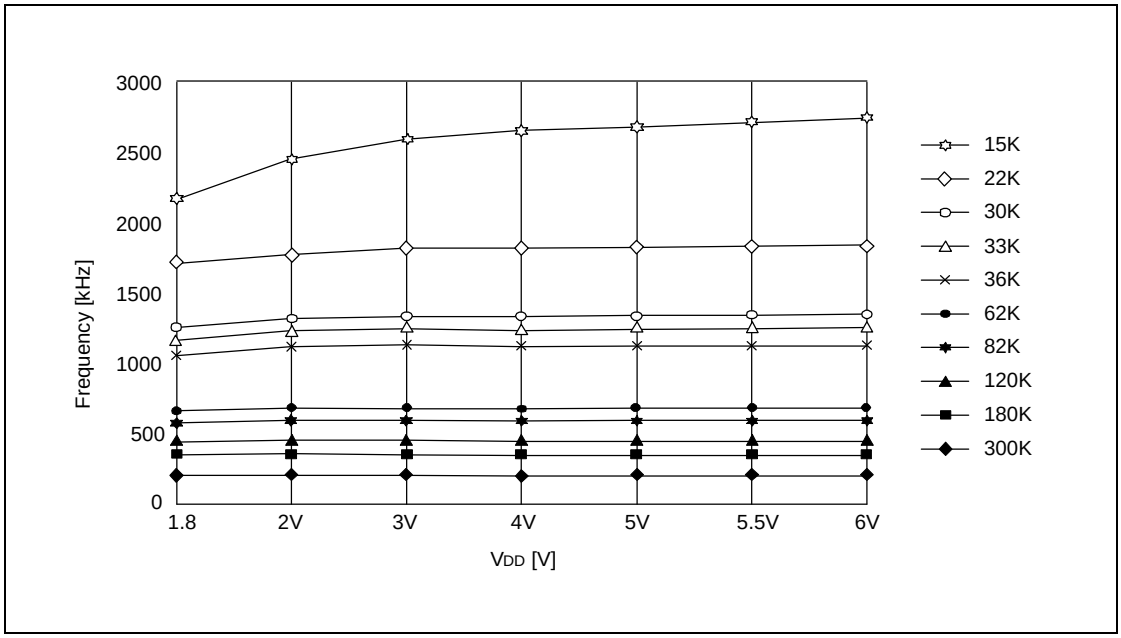


Figure 18-6. RC Oscillator Characteristic Curve

Table 18-7. Main Oscillator Oscillation Stabilization Time (t_{ST1})

(T_A = -40°C + 85°C, V_{DD} = 4.5 V to 5.5 V)

Oscillator		Test Condition(Normal mode)	Min	Typ	Max	Unit
HSX	Crystal	V_{DD} = minimum oscillation voltage range.	–	–	10	ms
	Ceramic		–	–	4	ms
	External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	50	–	–	ns
MSX	Crystal	V_{DD} = minimum oscillation voltage range.	–	–	100	ms
	Ceramic		–	–	50	ms
	External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	50	–	–	ns
LSX	32768Hz Crystal	V_{DD} = minimum oscillation voltage range.	–	200	500	ms

NOTE: Oscillation stabilization time (t_{ST1}) is the time that is required to stabilize oscillation after a reset or STOP mode release.

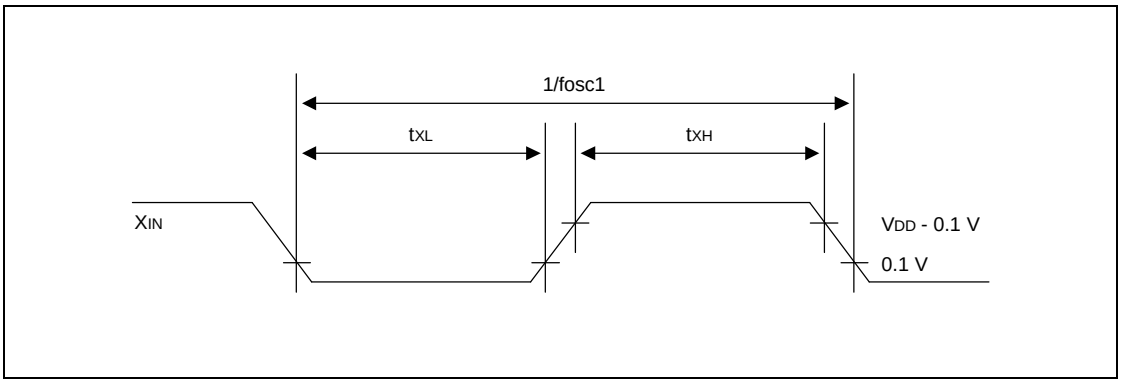
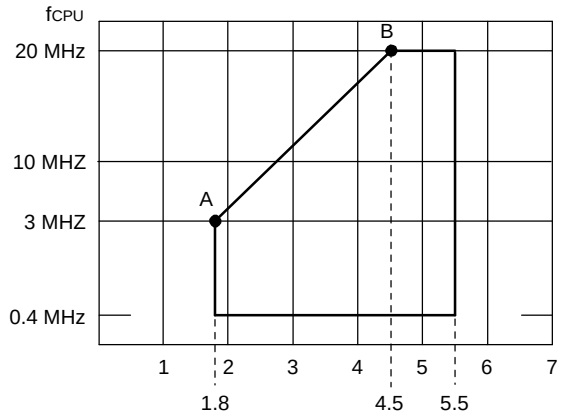
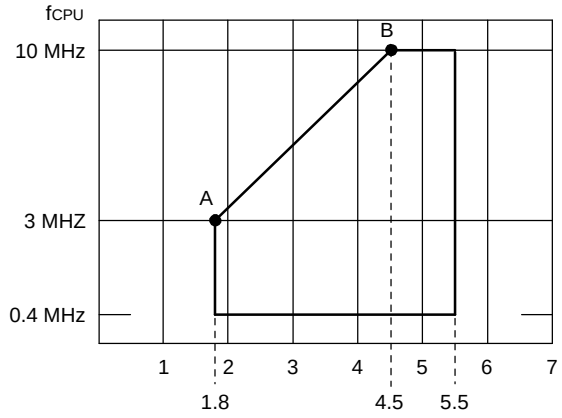


Figure 18-7. Clock Timing Measurement at X_{IN}



Minimum instruction clock = 1/1 x oscillator frequency

Figure 18-8. HSX Mode Operating Voltage Range



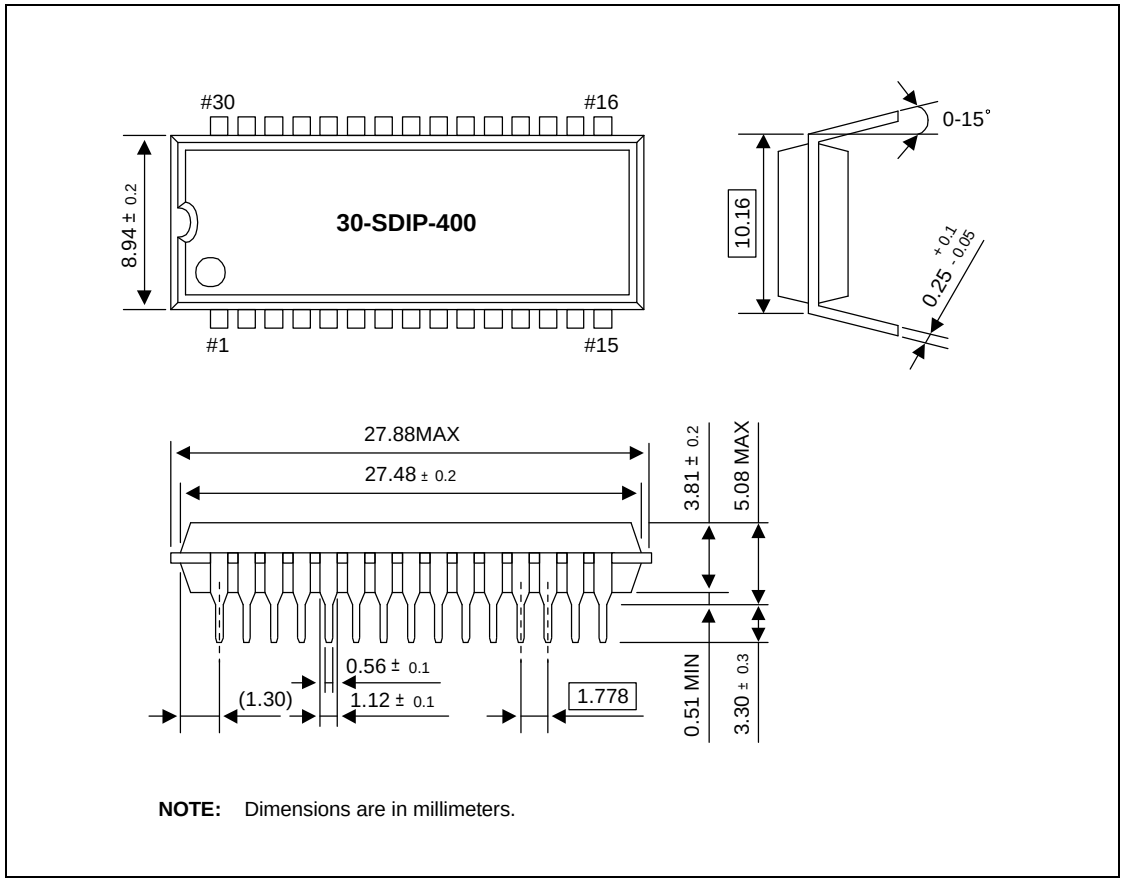
Minimum instruction clock = 1/1 x oscillator frequency

Figure 18-9. MSX Mode Operating Voltage Range

19 MECHANICAL DATA

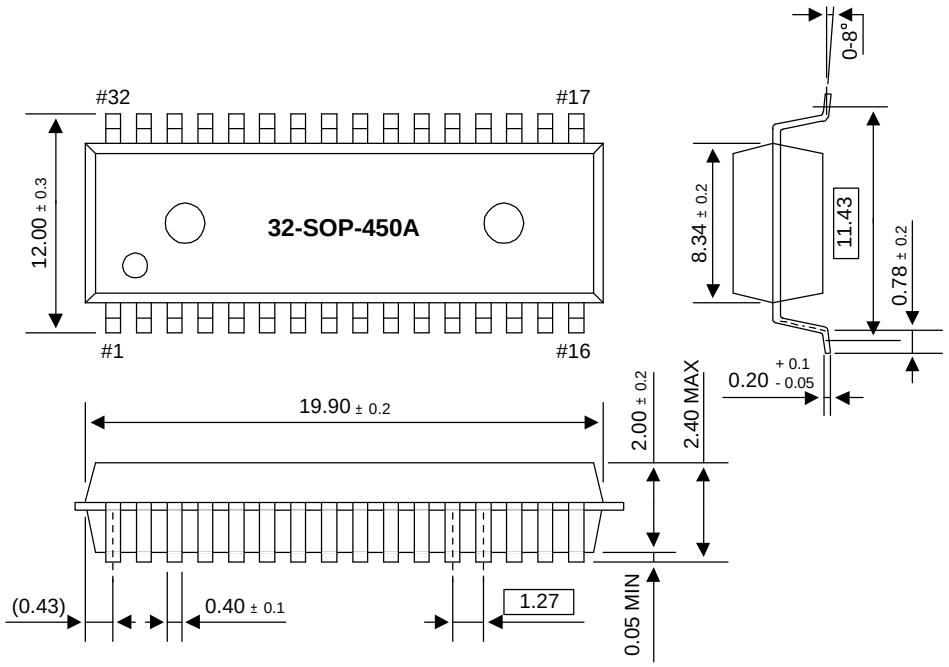
OVERVIEW

The S3CB018/FB018 is available in a 30-pin SDIP package (Samsung: 30-SDIP-400) and a 32-pin SOP package (32-SOP-450A). Package dimensions are shown in Figures 20-1 and 20-2.



NOTE: Dimensions are in millimeters.

Figure 19-1. 30-Pin SDIP Package Dimensions



NOTE: Dimensions are in millimeters

Figure 19-2. 32-SOP-450A Package Dimensions

20 S3FB018 FLASH MCU

OVERVIEW

The S3FB018 single-chip CMOS microcontroller is the FLASH version of the S3CB018 microcontroller. It has an on-chip FLASH ROM instead of masked ROM. The FLASH ROM is accessed in serial data format.

The S3FB018 is fully compatible with the S3CB018, both in function and in pin configuration. Because of its simple programming requirements, the S3FB018 is ideal for use as an evaluation chip for the S3CB018.

PIN ASSIGNMENTS

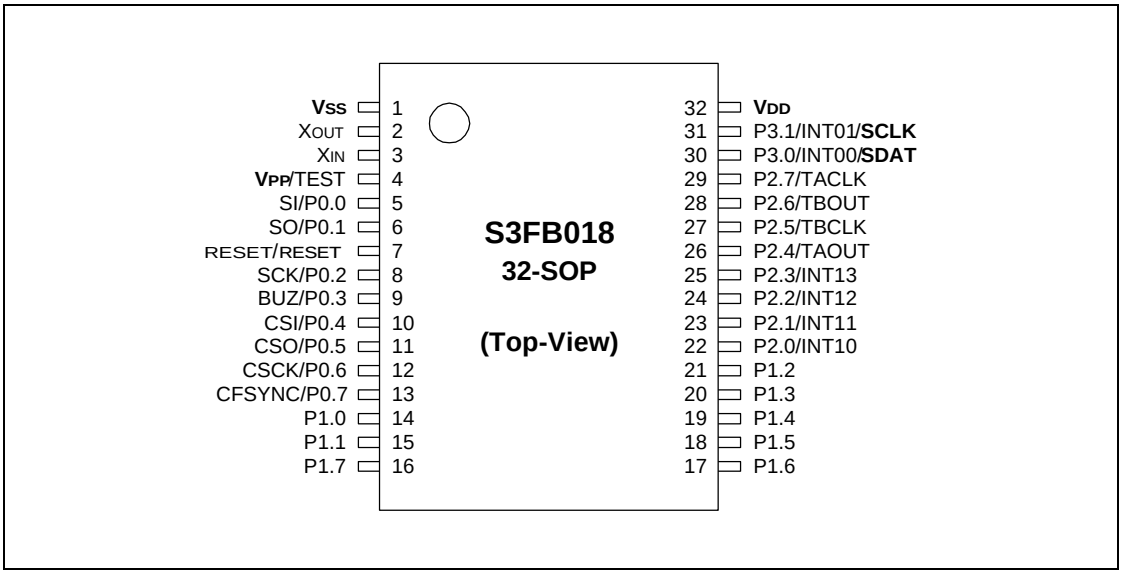


Figure 20-1. 32-SOP Pin Assignment

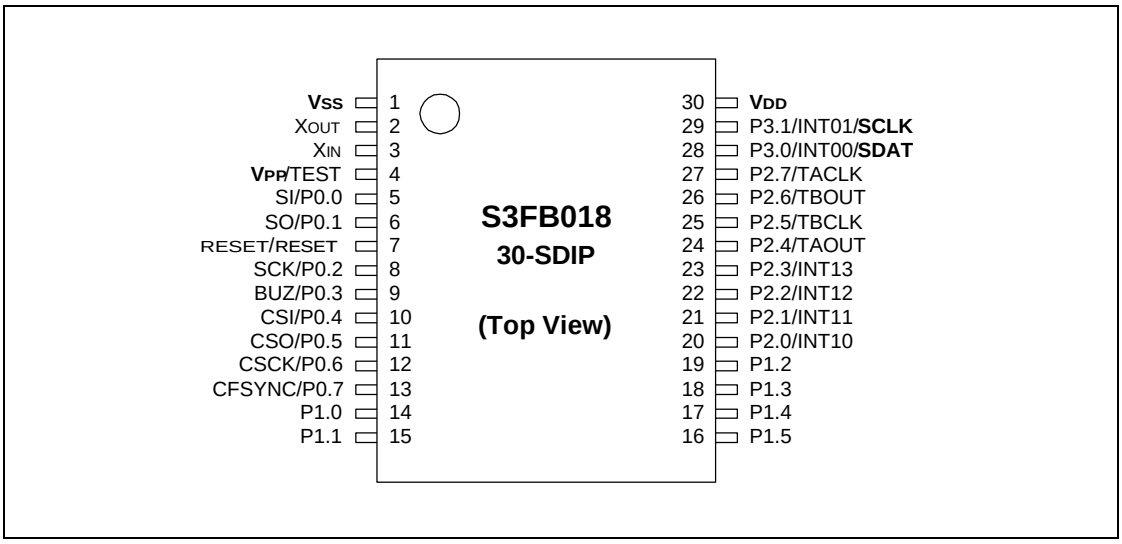


Figure 20-2. 30-SDIP Pin Assignment

Table 20-1. Descriptions of Pins Used to Read/Write the FLASH ROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P3.0	SDAT	30(28)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P3.1	SCLK	31(29)	I/O	Serial clock pin. Input only pin.
TEST	Vpp (TEST)	4	I	Power supply pin for FLASH ROM cell writing (indicates that FLASH enters into the writing mode). When 12.5 V is applied, FLASH is in writing mode and, when 5 V is applied, FLASH is in the reading mode. When FLASH is operating , hold GND.
RESET	RESET	7	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	32/1(30/1)	–	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: Pin No. is for 100 QFP type package. (for 100 TQFP, the pins with the same name have same functions).

Table 20-2. Comparison of S3FB018 and S3CB018 Features

Characteristic	S3FB519	S3CB519
Program Memory	4K word (8K byte) FLASH ROM	4K word (8K byte) FLASH ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	
Pin Configuration	32-SOP/30-SDIP	32-SOP/30-SDIP
FLASH ROM Programmability	User programmable	Programmed at the factory

Table 20-3. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	–0.3 to + 6.0	V
Input voltage	V_I	–	–0.3 to V_{DD} + 0.3	
Output voltage	V_O	–	–0.3 to V_{DD} + 0.3	
Output current high	I_{OH}	One I/O pin active	–18	mA
		All I/O pins active	–60	
Output current low	I_{OL}	One I/O pin active	+ 30	
		Total pin current for ports 1, 2, 3	+ 100	
Operating temperature	T_A	–	–40 to + 85	°C
Storage temperature	T_{STG}	–	–65 to + 150	

Table 20-4. D.C. Electrical Characteristics

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage (HSX mode)	V_{DD}	F_{CPU} = 20 MHz	4.5	–	5.5	V
		F_{CPU} = 3 MHz	1.8		5.5	
Operating Voltage (MSX mode)	V_{DD}	F_{CPU} = 10 MHz	4.5	–	5.5	
		F_{CPU} = 3 MHz	1.8		5.5	

Table 20-4. D.C. Electrical Characteristics (Continued)

(T_A = –40°C to +85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD}- 0.1			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	
	V_{IL2}	X_{IN}			0.1	
Output high voltage	V_{OH1}	V_{DD} = 5V; I_{OH} = -1 mA All output pins	V_{DD}-1.0	–	–	V
Output low voltage	V_{OL1}	V_{DD} = 5V; I_{OL} = 8 mA All output pins except V_{OL2}	–	–	2	
	V_{OL2}	V_{DD} = 5V; I_{OL} = 15 mA, Port 1			2	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	3	uA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, XT_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except I_{LIL2}	–	–	-3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, XT_{IN}, RESET			-20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and Output pins	–	–	3	uA
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and Output pins	–	–	-3	
Oscillator feed back resistors	R_{osc1} (HSX)	V_{DD} = 5.0 V, T_A = 25°C X_{IN} = V_{DD}, X_{OUT} = 0V	510	710	910	kΩ
	R_{osc2} (MSX)	V_{DD} = 5.0 V, T_A = 25°C X_{IN} = V_{DD}, X_{OUT} = 0V	510	710	910	
	R_{osc3} (LSX)	V_{DD} = 5.0 V, T_A = 25°C X_{IN} = V_{DD}, X_{OUT} = 0V	2.0	2.7	3.5	MΩ
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0,1,2,3,4,5 T_A=25°C	30	50	70	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% T_A=25°C, RESET only	110	210	310	

Table 20-4. D.C. Electrical Characteristics (Continued)

(T_A = –40°C to +85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (1)	I_{DD1}(2)	Operating mode: V_{DD} = 5 V ± 10% **20 MHz** crystal oscillator(HSX)	–	10	20	mA
		5 MHz crystal oscillator(MSX)		4	8	
		V_{DD} = 3 V ± 10% **5 MHz** crystal oscillator(MSX)		2	4	
	I_{DD2}(3)	Idle mode: V_{DD} = 5 V ± 10% **20 MHz** crystal oscillator(HSX)	–	2.5	5	mA
		5 MHz crystal oscillator(MSX)		1	2	
		V_{DD} = 3 V± 10% **5 MHz** crystal oscillator(MSX)		0.4	0.8	
	I_{DD3}	Stop mode V_{DD} = 5 V ± 10%	–	0.5	3	uA
		V_{DD} = 3 V ± 10%		0.2	1.2	

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. In operating current test mode Timer A and Timer B are running.
3. In idle current test mode the Watch timer is running.
4. The operating and idle currents are measured at weak mode.